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Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*	*Complete if Known* Application Number: 10/802,566 Filing Date: 03-17-2004 First Named Inventor:**MOU-SHIUNG LIN** Art Unit: 2892 Examiner Name**: AJAY ARORA**
Sheet **1** of **3**	Attorney Docket No: 085027-0109

US PATENT DOCUMENTS

Examiner Initial *	Cite No	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or RelevantFigures Appear
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FOREIGN PATENT DOCUMENTS

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		NONE				

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	MISTRY, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pgs. 247-250	
	2	EDELSTEIN, D.C., "Advantages of Copper Interconnects," Proceedings of the 12th International IEEE VLSI Multilevel Interconnection Conference (1995) pgs. 301-307	
	3	THENG, C. et al. "An Automated Tool Deployment for ESD (Electro-Static-Discharge) Correct-by-Construction Strategy in 90 nm Process," IEEE International Conference on Semiconductor Electronics (2004) pgs. 61-67	
	4	GAO, X. et al. "An improved electrostatic discharge protection structure for reducing triggering voltage and parasitic capacitance," Solid-State Electronics, 27 (2003), pgs. 1105-1110	
	5	YEOH, A. et al. "Copper Die Bumps (First Level Interconnect) and Low-K Dielectrics in 65nm High Volume Manufacturing," Electronic Components and Technology Conference (2006) pgs. 1611-1615	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AA/

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	6	HU, C-K. et al. "Copper-Polyimide Wiring Technology for VLSI Circuits," Materials Research Society Symposium Proceedings VLSI V (1990) pgs. 369-373	
	7	ROESCH, W. et al. "Cycling copper flip chip interconnects," Microelectronics Reliability, 44 (2004) pgs. 1047-1054	
	8	LEE, Y-H. et al. "Effect of ESD Layout on the Assembly Yield and Reliability," International Electron Devices Meeting (2006) pgs. 1-4	
	9	YEOH, T-S. "ESD Effects On Power Supply Clamps," Proceedings of the 6th International Sympoisum on Physical & Failure Analysis of Integrated Circuits (1997) pgs. 121-124	
	10	EDELSTEIN, D. et al. "Full Copper Wiring in a Sub-0.25 pm CMOS ULSI Technology," Technical Digest IEEE International Electron Devices Meeting (1997) pgs. 773-776	
	11	VENKATESAN, S. et al. "A High Performance 1.8V, 0.20 pm CMOS Technology with Copper Metallization," Technical Digest IEEE International Electron Devices Meeting (1997) pgs. 769-772	
	12	JENEI, S. et al. "High Q Inductor Add-on Module in Thick Cu/SiLK™ single damascene," Proceedings from the IEEE International Interconnect Technology Conference (2001) pgs. 107-109	
	13	GROVES, R. et al. "High Q Inductors in a SiGe BiCMOS Process Utilizing a Thick Metal Process Add-on Module," Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting (1999) pgs. 149-152	
	14	SAKRAN, N. et al. "The Implementation of the 65nm Dual-Core 64b Merom Processor," IEEE International Solid-State Circuits Conference, Session 5, Microprocessors, 5.6 (2007) pgs. 106-107, pg. 590	
	15	KUMAR, R. et al. "A Family of 45nm IA Processors," IEEE International Solid-State Circuits Conference, Session 3, Microprocessor Technologies, 3.2 (2009) pgs. 58-59	
	16	BOHR, M. "The New Era of Scaling in an SoC World," International Solid-State Circuits Conference (2009) Presentation Slides 1-66	
	17	BOHR, M. "The New Era of Scaling in an SoC World," International Solid-State Circuits Conference (2009) pgs. 23-28	
	18	INGERLY, D. et al. "Low-K Interconnect Stack with Thick Metal 9 Redistribution Layer and Cu Die Bump for 45nm High Volume Manufacturing," International Interconnect Technology Conference (2008) pgs. 216-218	

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	19	KURD, N. et al. "Next Generation Intel® Micro-architecture (Nehalem) Clocking Architecture," Symposium on VLSI Circuits Digest of Technical Papers (2008) pgs. 62-63	
	20	MALONEY, T. et al. "Novel Clamp Circuits for IC Power Supply Protection," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part C, Vol. 19, No. 3 (07-1996) pgs. 150-161	
	21	GEFFKEN, R. M. "An Overview of Polyimide Use in Integrated Circuits and Packaging," Proceedings of the Third International Symposium on Ultra Large Scale Integration Science and Technology (1991) pgs. 667-677	
	22	LUTHER, B. et al. "Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices," Proceedings of the 10th International IEEE VLSI Multilevel Interconnection Conference (1993) pgs. 15-21	
	23	MASTER, R. et al. "Ceramic Mini-Ball Grid Array Package for High Speed Device," Proceedings from the 45th Electronic Components and Technology Conference (1995) pgs. 46-50	
	24	MALONEY, T. et al. "Stacked PMOS Clamps for High Voltage Power Supply Protection," Electrical Overstress/Electrostatic Discharge Symposium Proceedings (1999) pgs. 70-77	
	25	LIN, M.S. et al. "A New System-on-a-Chip (SOC) Technology – High Q Post Passivation Inductors," Proceedings from the 53rd Electronic Components and Technology Conference (05-30-2003) pgs. 1503-1509	
	26	MEGIC CORP. "MEGIC way to system solutions through bumping and redistribution," (Brochure) (02-06-2004) pgs. 1-3	
	27	LIN, M.S. "Post Passivation Technology™ - MEGIC ® Way to System Solutions," Presentation given at TSMC Technology Symposium, Japan (10-01-2003) pgs. 1-32	
	28	LIN, M.S. et al. "A New IC Interconnection Scheme and Design Architecture for High Performance ICs at Very Low Fabrication Cost – Post Passivation Interconnection," Proceedings of the IEEE Custom Integrated Circuits Conference (09-24-2003) pgs. 533-536	

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